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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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09/742,250

12/20/2000

Carl Werner

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20306

7590

12/04/2002

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EXAMINER

NGUYEN, LINH V

ART UNIT

PAPER NUMBER

2819

DATE MAILED: 12/04/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

AK

<b>Office Action Summary</b>	Application No. 09/742,250	Applicant(s) WERNER ET AL.	
	Examiner Linh V. Nguyen	Art Unit 2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 9/25/02.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-23 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-7, and 9-23 is/are rejected.
- 7) ☒ Claim(s) 8 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 20 December 2000 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on \_\_\_\_\_ is: a) ☐ approved b) ☐ disapproved by the Examiner.  
If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. §§ 119 and 120**

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
a) ☐ All b) ☐ Some \* c) ☐ None of:  
1. ☐ Certified copies of the priority documents have been received.  
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).  
\* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).  
a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

**Attachment(s)**

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)                  | 4) <input type="checkbox"/> Interview Summary (PTO-413) Paper No(s). _____  |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)         | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ | 6) <input type="checkbox"/> Other: _____                                    |

***Response to Amendment***

1. This office action is in response to applicant's amendment received on 10/16/02. Claims 1 – 14, and 16 – 20, have been amended. Claims 21- 23 have been added. Claims 1 – 23 are pending on this application.

***Claim Rejections - 35 USC § 102***

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1, 2, 3, 4, 7, 9, 10, 11, 12, 13, 14, 15, 20, 21 and 22 are rejected under 35 U.S.C. 102(b) as being anticipated by Cummins U.S. patent No. 5,570,090.

4. Regarding to claims 1, 2, 3, 4, 7, 9, and 10 Cummins disclose an current mode driver DAC circuit (Fig. 7A, 7B) to provide an output that falls within a predetermined range (Fig.8), circuit comprising the steps of: sensing at least one of a process condition, a voltage condition and a temperature condition (Col. 5 lines 55 - 56); adjusting a full scale current of a DAC in accordance with the sensing step and setting a current control signal based on an output of the DAC (Fig. 8, Also see table 1 at line 11 of Col. 6); wherein

- the step of adjusting the full scale current comprises the steps of: generating an adjustment signal (Fig. 7B 'SYNC') in response to the sensing step; and

applying the adjustment signal to the current mode driver, the adjustment signal causing the current mode driver to adjust the full scale current (See Table 1)

- the step of applying the adjustment signal to the current mode driver comprises applying at least one predetermined voltage to a corresponding at least one transistor switch (Fig. 8, Table 1)

- the current control signal comprises a plurality of bits (Fig. 7B 'SYNC', 'TRISYNC')

- the sensing step comprises sensing a voltage/temperature sensitive DC parameter and AC parameter; applying a voltage/temperature independent current to a voltage/temperature load and detecting a voltage drop across the voltage/temperature load (Fig. 7A,7B).

5. Regarding to claim 20, the step in the claimed method are deem to be made clearly inherent by the predetermined threshold voltage as applied to claim 3 above by Cummins.

6. Claims 1, 2, 3, 4, 7, 9, 10, 11, 12, 13, 14, 15, 16, 18, and 20 are rejected under 35 U.S.C. 102(b) as being anticipated by Koyama et al. U.S. patent No. 5,570,582.

7. Regarding to claims 1, 2, 3, 4, 7, 9 and 10, Koyama's Fig. 1 disclose an current mode driver DAC circuit to provide an output (41) that falls within a predetermined range ( $V_{ref}$ ), the circuit comprising the steps of: sensing at least one of a process condition, a voltage condition and a temperature condition (Col. 3 lines 38 – 39); adjusting a full

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scale current of a DAC in accordance with the sensing step (Col. 6 lines 30 – 33) and setting a current control signal based on an output of the DAC (36); wherein

- the step of adjusting the full scale current comprises the steps of: generating an adjustment signal (switch A is closed) in response to the sensing step; and applying the adjustment signal to the current mode driver (switch A is open), the adjustment signal causing the current mode driver to adjust the full scale current (Col 8 lines 14 – 30)
- the step of applying the adjustment signal to the current mode driver comprises applying at least one predetermined voltage to a corresponding at least one transistor switch (Fig. 1)
- the current control signal comprises a plurality of bits (36)
- the sensing step comprises sensing a voltage/temperature sensitive DC parameter and AC parameter (inherent to the system, because AC component and DC component are integrated in the circuit); applying a voltage/temperature independent current to a voltage/temperature load (R) and detecting a voltage drop across the voltage/temperature load (Feedback ).

8. Regarding to claim 11, 12, 13, 14, and 15, Koyama et al. as applied to claims 1, 2, 3, 4, 7, 9 and 10 above, disclose every aspect of applicant's claimed invention.

9. Regarding to claim 16, and 18 wherein the step of calibrating the output driver comprises deriving the second output from as signal provided directly by the output driver (feedback) and apply to a transconductances stage (34).

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10. Regarding to claim 20, the step in the claimed method are deem to be made clearly inherent by the predetermined threshold voltage as applied to claim 3 above by Koyama et al.
11. Regarding to claim 21, and 22 wherein the current mode driver is a multi-level-amplitude modulation (Fig. 4), and the adjusting and setting steps occur in response to a triggering event after power up (Fig. 1 [17, 18, 19])

***Claim Rejections - 35 USC § 103***

12. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

13. Claim 5 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cummins or Koyama et al., in view of Hicks U.S. patent No. 6,015,233.

Cummins or Koyama et al. as applied to claim 1 above, disclose every aspect of applicant's claimed invention, however Cummins is silent to the sensing step comprises determining a condition associated with a delay-locked loop or a phase-locked loop.

Fig. 5 Gillig teaches a temperature-sensing system comprises determining a condition associated with a phase-locked loop or a delayed-locked loop (Col. 4 line 62 – Col. 5 line10).

Cummins or Koyama et al. and Gillig are analogous, because they are from a similar problem solving area of voltage/temperature sensing circuit. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to apply the locked-loop circuit of Gillig's sensing-circuit to the sensing-circuit of Cummins et al. for the purpose of providing accurate, linear and repeatable temperature compensation with more simplified circuitry (Col. 2 lines 1 – 4).

14. Claims 17, and 19, are rejected under 35 U.S.C. 103(a) as being unpatentable over Koyama et al.

Regarding to claims 17, and 19, Koyama et al. as applied to claim 18 above disclose every aspect of claimed invention except for applying the second output resistive divider or switch capacitor.

15. Claim 15 generic to a plurality of disclosed patentably distinct species comprising transconductances, or resistive divider, or switched capacitor circuit (Claims 17, 18, 19). Applicant has not disclosed that resistive divider or switched capacitor or transconductances, provides an advantage, is used for a particular purpose, or solves a stated problem, over one to other. One ordinary skill in the art, furthermore, would have expected applicant's invention (switch capacitor or resistive divider circuit) to perform equally well with transconductances of Koyama et al. as applied to claim 18 above. Because, regarding claims 17, 18, and 19 applicant has shown three distinct invention are perform equally well with each other.

16. Claim 22 is rejected under 35 U.S.C. 103(a) as being unpatentable over Cummins or Koyama et al., in view Opris U.S. patent No. 6,130, 632.

Koyama et al as applied to claim 21 above disclose every aspect of applicant's claimed invention except for wherein the sensing, adjusting and setting steps occur in during a power up sequence.

Opris Fig. 5 discloses a digital self-calibrating current mode D/A converter having calibration procedure is performed upon power up or user request (Abstract).

Opris and Koyama are analogous, because they both relating to calibration for current mode D/A converter. Therefore it would have been obvious to one having ordinary skill in the art at the time the invention was made to apply calibrate by power-up or user request from the teaching of Opris' current mode, to calibration of Koyama' current mode for the purpose of providing flexibilities of calibration, as has suggested by Opris.

### ***Response to Arguments***

17. Applicant's arguments under remarks with respect to "current mode driver", "full scale output", "voltage and temperature condition ", have been considered but are moot in view of the new ground(s) of rejection (Specifically Cummins, Koyama et al., and Opris are now used to reject the claims as noted supra.

18. Applicant's argument under remarks with respect "high resolution". Examiner respectfully traverse, because the phrase "high resolution" is a state of quality or advantages of any circuit or device, it does not have any limitation or subject matter to claimed invention.



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19. Regarding to applicant's argument under remark with respect to claims 5 and 6 in combination of Gill. Examiner respectfully traverse, because Gill taught a sensing circuit using phase-lock-loop/delayed-lock-loop for the purpose of providing accurate, repeatable temperature compensating output. Therefore it would have been obvious to one in the art to apply with the temperature sensing circuit of Gill to the temperature sensing circuit of Cummins or Koyama et al..

***Allowable Subject Matter***

20. Claim 8 objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

***Contact Information***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Linh Van Nguyen whose telephone number is (703) 305-1934. The examiner can normally be reached from 8:30 – 5:00 Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mr. Michael Tokar can be reached at (703) 305-3493. The fax phone numbers for the organization where this application or proceeding is assigned

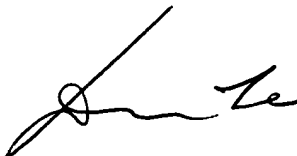
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are (703) 308-7722 for regular communications and (703) 308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

LVN

November 27, 2002

  
DON LE  
PRIMARY EXAMINER  
11/02/02